Contents

1 REYLOGIC

The purpose of ReyLogiC is to enable a high degree of flexibility within a relay. It allows elements within the relay to be interconnected with combinational logic, timers, counters and latches.

All timers and counters entered on a schematic diagram can be set within ReyLogiC to have a fixed setting which can only be modified from the ReyLogiC diagram editor or a visible setting which appears in the normal settings list to allow on site modifications without having to use a PC to modify schematics. All Boolean points marked as inputs on the schematic package appear in the settings lists by means of their 'tag name' with a matrix setting which allows that input to be driven from any of the status inputs. All Boolean points marked on the schematic package as outputs appear in the settings list by means of their 'tag name' with a matrix setting which allows any combination of output relays and fascia flags to be selected.

ReyLogiC is a Windows based schematic capture program which allows the manufacturer or a customer to enter a logical diagram using any number of logic elements which expresses the configuration of a particular function. The primary output of the package is a set of Boolean logic equations which can be downloaded into the relay. Other features include :-

- Loading and Saving of logic schematics
- Printing of logic schematics
- Generation of logic equations from schematics
- Printing of logic equations
- Connection to relay and download of schemes to relay.
- Cutting and Pasting to other windows applications for documentation purposes.
- Project management facilities for grouping logic diagrams as an overall assembly for download to relay along with supplemental files specifying default configurations for status input marshalling, output relay marshalling, IEC870 event codes etc.

Logic scripts are down loaded from the PC over the serial communications port using an ASCII protocol, each character received by the relay is echoed back to the PC to confirm correct transmission. If the logic script is not successfully transmitted the script will not be used by the relay.
The unit will attempt to run the last logic script to be loaded. To make a new logic script active following down loading the relay must be 'cold started', this mechanism is part of the ReyLogiC application after successful logic scheme transfer.
If the latest logic script is found to be invalid, or the unit has no logic scripts loaded when it is powered up the LCD will display 'NO LOGIC'
.
The following block diagram shows the logic execution engine for the IOTA.

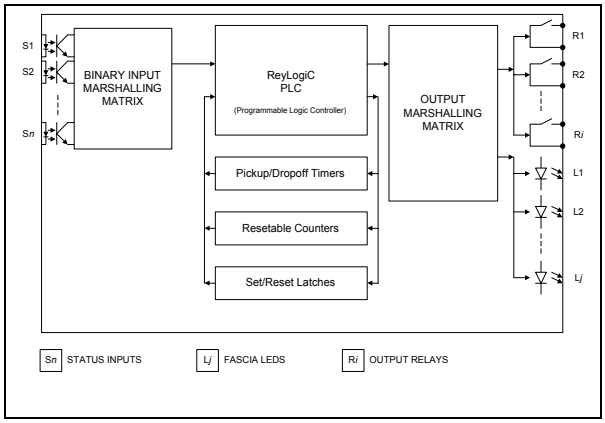
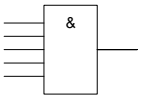


Figure 1: IED Block Diagram

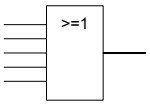
1. Logic Schematics Elements

.1. AND Gates



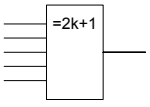
This is a multi-input logical AND gate. It takes as inputs the Boolean conditions which are wired to the inputs and outputs a Boolean which is the logical "AND". If all inputs are TRUE (Logical 1) then the output will be TRUE otherwise the output will be FALSE (Logical 0).
The number of inputs to each gate is adjustable upto 16 inputs.

.2. OR Gates



This is a multi-input logical OR gate. It takes as inputs the Boolean conditions which are wired to the inputs and outputs a Boolean which is the logical "OR". If one or more of the inputs is TRUE (Logical 1) then the output will be TRUE otherwise the output will be FALSE (Logical 0).
The number of inputs to each gate is adjustable upto 16 inputs.

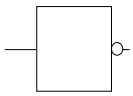
.3. XOR Gates



This is a double input logical XOR gate. It takes as inputs the Boolean conditions which are wired to the inputs and outputs

a Boolean which is the logical "XOR". If only one of the inputs is TRUE (Logical 1) then the output will be TRUE otherwise (both inputs TRUE or both inputs FALSE) the output will be FALSE (Logical 0).

.4. NOT Gates



This is a single-input NOT gate. The output Boolean condition is the logical NOT of the input Boolean. If the input is TRUE (Logical 1) then the output will be FALSE (Logical 0). If the input is FALSE (Logical 0) then the output will be TRUE (Logical 1).

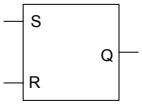
.5. Pickup / Drop off Timers

If the Boolean input remains TRUE for the entire PICK-UP time, the output Boolean will then also be set to TRUE. The output Boolean will remain TRUE as long as the Input Boolean also remains TRUE. When the input Boolean is set FALSE then the Output Boolean will also be set FALSE when the DROP-OFF timer expires.

.6. Resetable Counters

The resetable counters may be used to count discrete events. Every time the INPUT (C) transitions from a FALSE to a TRUE logical state the counter is incremented. When the specified terminal count is reached the OUTPUT is set to logical TRUE. If the RESET input becomes logically TRUE then the counter is zeroed and the OUTPUT is set FALSE and will remain held in this state until the RESET input condition reverts to FALSE.

.7. Set/Reset Latches



When the SET (S) input alone is logically TRUE then the OUTPUT (Q) is set logically TRUE. If the RESET (R) input is TRUE then the output will always be FALSE.

.8. Inputs

Boolean inputs to the logic system may belong to the output from another logic diagram or may be connected to a status input via the marshalling matrix. The 'tag name' given to the input on the ReyLogic diagram is used as the identification label found in the status input configuration menu.

.9. Outputs

Boolean outputs from the logic system may be an input to another logic diagram or may be connected to the output relay or fascia LED's via a marshalling matrix. The 'tag name' given to the output on the ReyLogic diagram is used as the identification label found in the output relay configuration menu.

2. SCHEME DESIGN

Reylogic gives the programmer the flexibility to ensure all control requirements are met within the logic scheme e.g. duration of output pulses, double pole inputs and don't believe it logic.

When using timers consideration must be given to the status input pick up/drop off delay and processing/scanning time of the logic (see Performance Specification).

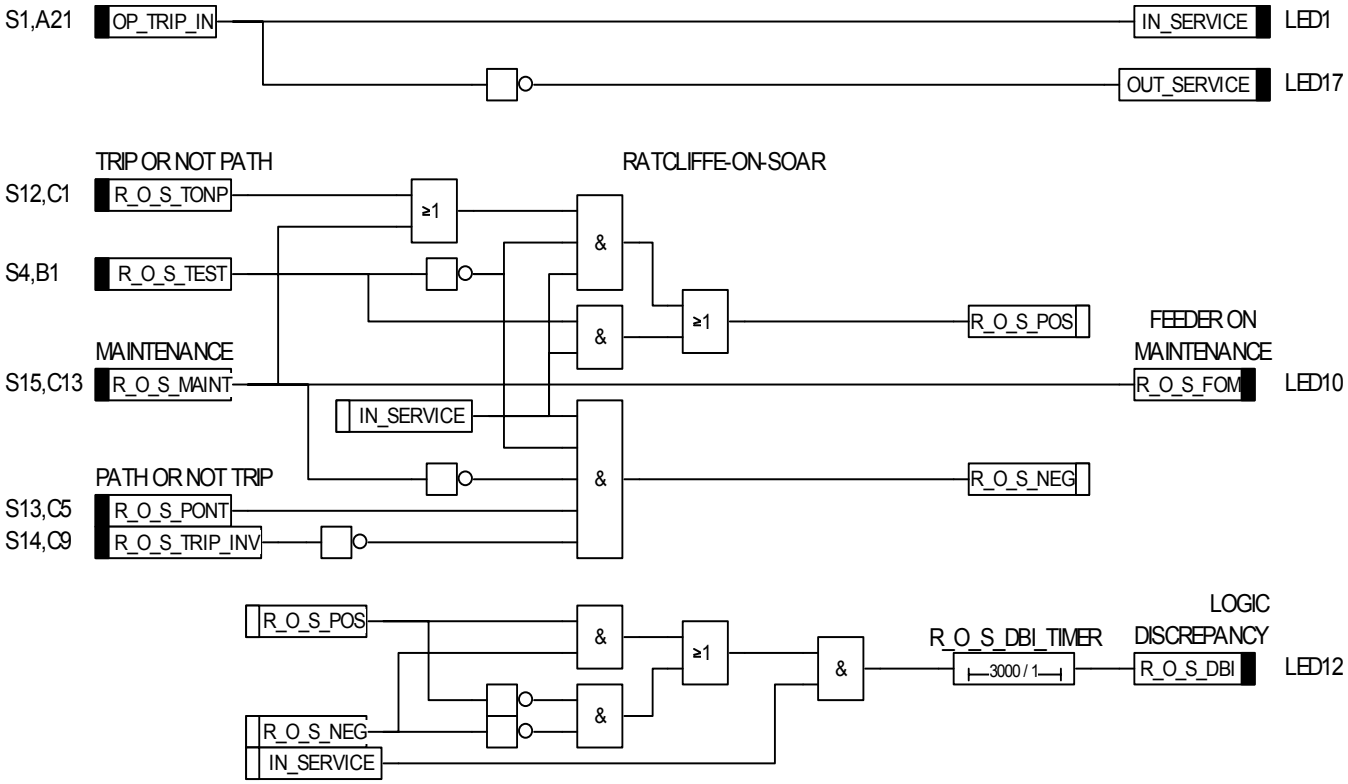


FIGURE 2: TYPICAL EXAMAPLE OF REYLOGIC SCHEME DIAGRAM